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Design and Analysis of Sequential Elements for Low Power Clocking System with Low Power Techniques

[1]S.Sasidhar Reddy [2]B.Shoban Babu
Electronics&Communication Engineering, M.Tech Student, SVCET (Autonomous) Chittoor, India
Electronics&Communication Engineering, Associate professor, SVCET (Autonomous) Chittoor, India

ABSTRACT:
This paper proposed the design of sequential elements for low power clocking system with low low power techniques for saving the power. Power consumption is a major bottleneck of system performance and is listed as one of the top three challenges in International Technology Roadmap for Semiconductor 2008. In practice, a large portion of the on chip power is consumed by the clock system which is made of the clock distribution network and flop-flops. In this paper, various design techniques for a low power clocking system are surveyed. Among them is an effective way to reduce capacity of the clock load by minimizing number of clocked transistors. To approach this, proposed a novel clocked pair shared flip-flop which reduces the number of local clocked transistors by approximately 40%. A 24% reduction of clock driving power is achieved. In addition, low swing and double edge clocking, can be easily incorporated into the new flip-flop to build clocking systems. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is off. Dual sleep and sleepy stack methods are proposed to avoid static power consumption; the flip flops are simulated using HSPICE.
KEYWORDS: Avg power, Dual sleep, Flip-flops, low power, Sleepy stack

I. Introduction

The system on chip (SoC) design is integrating hundreds of millions of transistors on one chip, whereas packaging and cooling only have a limited ability to remove the excess heat. All of these results in power consumption being the bottleneck in achieving high performance and it is listed as one of the top three challenges in ITRS 2008 The clock system, which consists of the clock distribution Network and sequential elements (flip-flops and latches), is one of the most power consuming components in a VLSI system [1], [2]. There is a wide selection of flip-flops in the literature [1]–[18].Many contemporary microprocessors selectively use master-slave and pulsed-triggered flip-flops [2]. Traditional master-slave single-edge flip-flops, for example, transmission gated flip-flop [3], are made up of two stages, one master and one slave. Another edge-triggered flip-flop is the sense amplifier-based flip-flop (SAFF) [4]. All of these hard edged-flip-flops are characterized by a positive setup time, causing large D-to-Q delays. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. 95% of all static timing latching on the Itanium 2 processor use pulsed clocking [5]. Pulse triggered flip-flops could be classified into two types, implicit-pulsed and explicit-pulsed, for example, the implicit pulse-triggered data-close-to-output flip-flops (ip-DCO) [6] and the explicit pulse-triggered data-close-to-output flip-flops (ep-DCO) [6].

In CMOS integrated circuit design there is a trade-off between static power consumption and technology scaling. Recently, the power density has increased due to combination of higher clock speeds, greater functional integration, and smaller process geometries. As a result static power consumption is becoming more dominant.

CMOS technology feature size and threshold voltage have been scaling down for decades for achieving high density and high performance. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power [7].

II. Survey of low power design

Power consumption is determined by several factors including frequency f, supply voltage V, data activity α capacitance C, leakage, and short circuit current

$$P = P_{dynamic} + P_{short\ circuit} + P_{leakage} \quad (1)$$

$P_{short\ circuit}$ power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short while.

$P_{leakage}$ is the leakage power. With supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the sub threshold leakage current. Sub threshold leakage is the dominant leakage now $P_{leakage} = \mathbf{I}_{leakage}\mathbf{V}_{dd}$.

Various ways to lower the power consumption are a) Double Edge Triggering [8] by reducing frequency in equation b) low swing voltage on a clock distribution network [9] by reducing voltage in a equation c) Conditional Operation example conditional discharge flip flop (CDFF) [10] and conditional discharge flip flop [11] by reducing the redundant switching activities or d)clock gating [12] methods by reducing switching activity e) Reducing short circuit power by splitting short circuit power f)Reducing capacity of clock load because clocked nodes have 100% activity g)Dual Vt/MTCMOS to reduce the power in stand by mode by reducing leakage power[13].

III. Reducing clock capacity by minimizing the number of clocked transistors

A large part of the on-chip power is consumed by the clock drivers [14]. It is desirable to have less clocked load in the system. For the minimization of clocked transistors and measuring the power we have studied Conditional Capture Flip Flop(CCFF) [11],Conditional Discharge Flip Flop(CDFF)[10] ,Conditional Data Mapping Flip Flop(CDMFF)[19],Clock Pair Shared Flip Flop(CPFF).

3.1 Conditional Discharge Flip Flop

Conditional Discharge Flip flop [10] have 15 clocked transistors, compared to another flip flops such as CCFF, CDMFF, CPSFF it is more number so it takes more power consumption. The extra switching activity is eliminated by controlling the discharge path when the input is stable high and, the name Conditional Discharge technique.

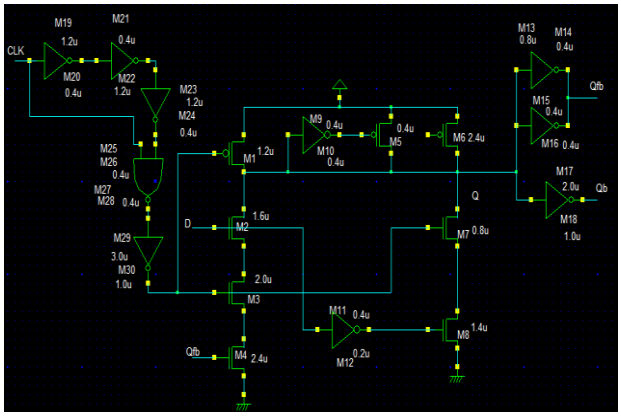

Fig.1. Conditional Discharge Flip Flop

Above" Fig.1" consists the pulse generator which is suitable for double edge sampling and it consists two stages, they are X and Y for capturing the input data in correct manner. Stage one is responsible for capturing the LOW to HIGH transition, as a result the output node will be charged to HIGH through M4 in the Second stage. If the input D is HIGH in the sampling window, the internal node X is discharged, assuming that (Q,Qb) were initially (LOW, HIGH) for the discharge path to be enabled. As a result, the output node will be charged to HIGH through M6 in the second stage. Stage 2 captures the HIGH-to-LOW input transition. If the input D was LOW during the sampling period, then the first stage is disabled, and node retains its precharge state. Whereas, node Y will be HIGH, and the discharge path in the second stage will be enabled in the sampling period, allowing the output node to discharge and to correctly capture the input data.

3.1.1 Simulation result of CDFF

The CDFF circuit is simulated in HSPICE at level 68 with L=0.18u

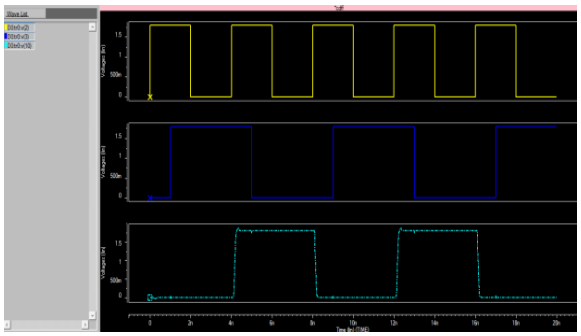

Fig.2 Conditional Discharge Flip Flop output wave form

3.2 Conditional Capture Flip Flop

Conditional Capture Flip flop [11] has 14 clocked transistors. This technique is based on the clock gating Idea.CCFF produces transparent window for sample the input and this produces by implicit pulse generator. The Delayed version of CLKD is used to de Couple the input as in differential structure. When D

is at a low logic value, M9 turns on, and Q stays at or is pulled down to the ground. Once transitions low by the pull-up of the delayed version of CLKD the clock , the node X is decoupled from the input as in the differential structure .Q is also decoupled from when DB becomes low. At the falling edge of the clock,X is precharged to or held at the supply voltage and stay there as long as the clock remains low

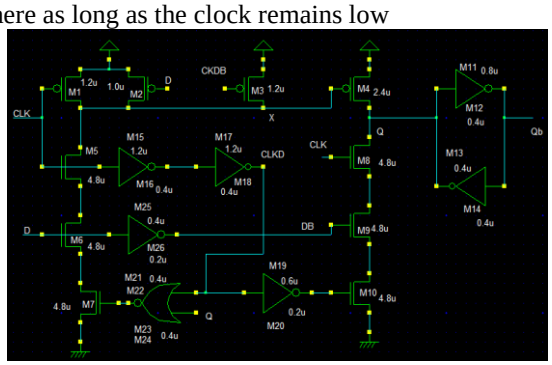

Fig.3 Conditional Capture Flip Flop

3.2.1 Simulation result of CCFF

The CCFF circuit is simulated in HSPICE at level 68 with L=0.18u

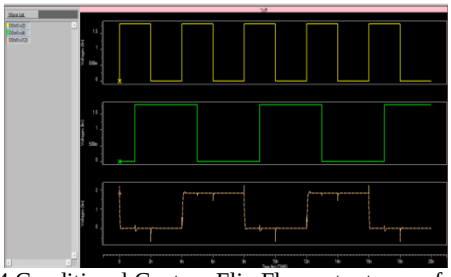

Fig.4 Conditional Capture Flip Flop output wave form

3.3 Conditional Data Mapping Flip Flop

Dynamic Power is reduced by mapping their inputs to a configuration that eliminate the redundant internal transitions. CDMFF [15] consist the 14 clocked transistors. When a CLK transits from 0 to 1, CLKDB will stay 1 for a short while which produces implicit window for evaluation. This creates a floating node problem.

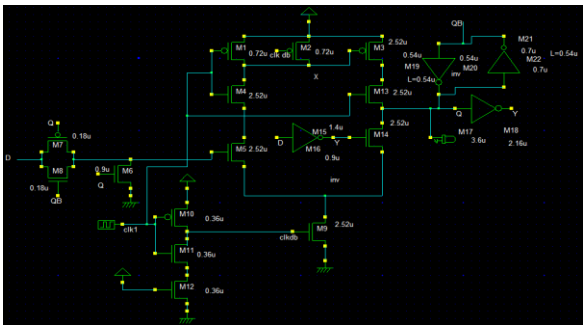

Fig.5 Conditional Data Mapping Flip Flop

3.3.1 Simulation result of CDMFF

The CDMFF circuit is simulated in SPICE at level 68 with L=0.18u

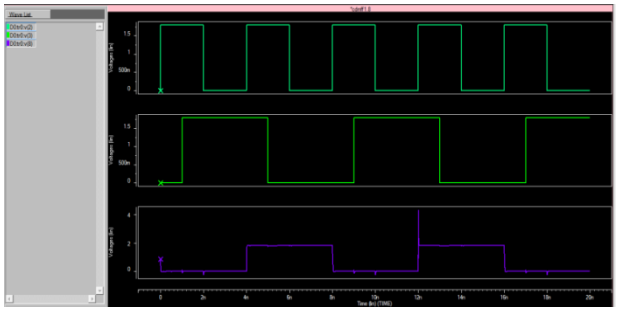

Fig.6 Conditional Data Mapping Flip Flop output wave form

3.3.2 Floating node problem

During that window, both M1,M2 are off, when D 0 or 1 then at X floating node Occur i.e. neither 0 nor 1.8v.If a nearby noise discharges the node X, M3 partially on and glitch will appear on output node Q.

Fig.7 Conditional Data Mapping Flip Flop floating problem wave form

Data is 1.8v but at node X the floating occurring i.e 4v is measured. This Floating node makes the glitch at the Output .Glitch not only consumes the more power but also more vulnerable to noise. Hence CDMFF could not be used In noise intensive environment. Clock structure with precharging transistors M1 and M2 in CDMFF makes it difficult to apply double edge triggering.

3.4 Clock pair Shared Flip Flop

The clock pair (M_4, M_5) is shared between second stage and first stage in. An always on PMOS, M1 is used to charge the internal node X rather than using the two clocked precharging transistors (M_1, M_2) in CDMFF.

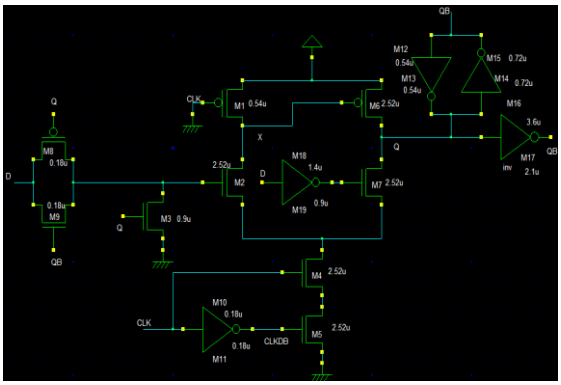

Fig.8 Clock Pair Shared Flip Flop

3.4.1 Simulation result of CPSFF

The CPSFF circuit is simulated in HSPICE at level 68 with L=0.18u

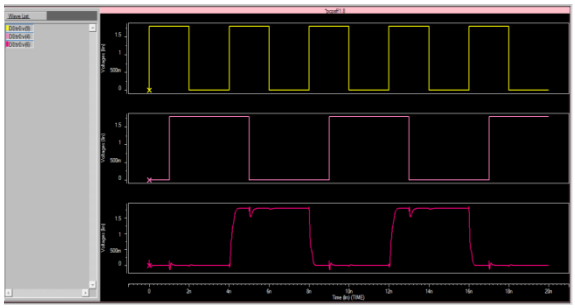

Fig.9 Clock Pair Shared Flip Flop Wave form

3.4.2 No Floating node problem

The internal node X is connected to Vdd by an always on M1, so is not floating, resulting in enhancement of noise robustnessof node X. This solves the floating point problem in CDMFF that is Output is 1.8v

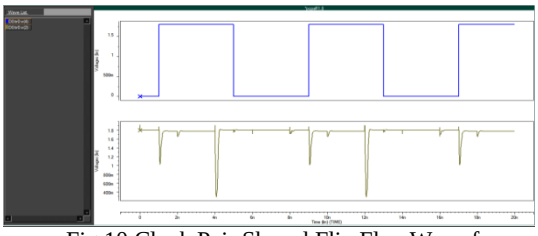

Fig.10 Clock Pair Shared Flip Flop Wave form

IV. Comparing the flip-flops

The simulation results were obtained from HSPICE simulations in 0.18um CMOS technology at room temperature. VDD is 1.8 V. we have simulated the circuits in a real environment, where the flip-flop inputs (clock, data) are driven by the input buffers, and the output is required to drive an output load. An inverter is placed after output Q, providing protection from direct noise coupling [6].In order to calculate the delay COSMOSCOPE is used.

Table 1
Comparing the flip-flop in terms of delay, power, and power delay product

Flip Flop	Clock Transistors	Delay	power	Power delay Product (fJ)	% of power saving
CDFF	15	3.16	91.56	289.32	0
CCFF	14	3.04	90.86	276.21	0.76
CDMFF	7	3.06	83.96	256.91	8.30
CPSFF	4	3.125	79.80	249.37	12.84

The proposed clocked-pair shared flip-flop is more efficient than other designs like the CCFF, CDFF, and CDMFF. It uses the least number of clocked transistors and saves 12.84% of power

V. Proposed Low power techniques

In CMOS integrated circuit design there is a trade-off between static power consumption and technology scaling. Recently, the power density has increased due to combination of higher clock speeds, greater functional integration, and smaller process geometries. As a result static power consumption is becoming more dominant. This is a challenge for the circuit designers. However, the designers do have a few methods which they can use to reduce this static power consumption. In order to achieve lower static power consumption; one has to sacrifice design area and circuit performance

As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique. There are two techniques for to reduce the leakage power they are Dual sleep and sleepy techniques. Stack techniques [7].These techniques applied for both conditional data mapping flip flop (CDMFF) “Fig .5”and clock pair shared flip flop (CPSFF)

5.1 CDMFF Dual Sleep Approach

Dual sleep [16] approach uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit.

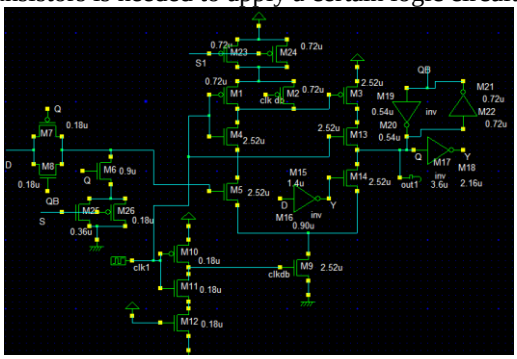

Fig.11 CDMFF Dual Sleep

In CDMFF Dual sleep approach flip flop the extra transistors 4(M23,M24,M25,M26) in pull up and pull down are arranged for conventional CDMFF flip flop .The W/L ratios are maintained for achieving correct output.S,S1 are control switches to maintain

the output. The power is saved compared to the conventional CDMFF.

5.1.1 Simulation result of Dual Sleep CDMFF
The CDMFF dual sleep circuit is simulated in HSPICE at level 64 with L=0.18u

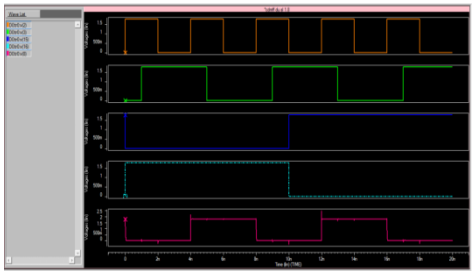

Fig.12 Dual Sleep CDMFF Wave form

5.2 CDMFF Sleepy stack Approach

The sleepy stack [7] approach combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach[17]. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. The extra pair are arranged in pull up mode (M23, M24) and another

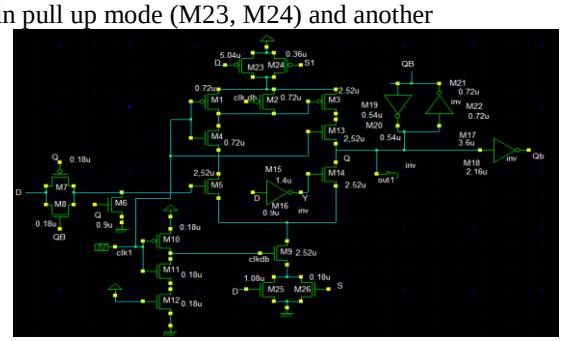

Fig.13 CDMFF Sleepy Stack

5.2.1 Simulation result of Sleepy Stack CDMFF
The CPSFF sleepy stack circuit is simulated in HSPICE at level 64 with L=0.18u

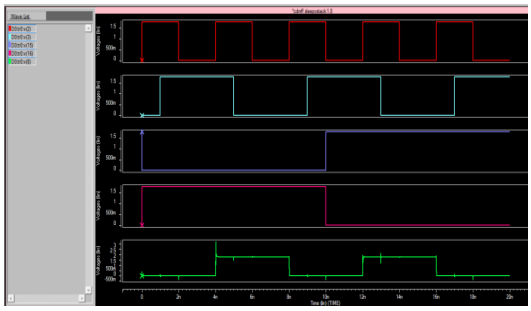

Fig.14 Sleepy Stack CDMFF output Wave form

5.3 CPSFF Dual Sleep Approach

In CPSFF dual sleep [16] approach the pmos and nmos are parallel to each other in pull up section and also Pull down network .The circuit is works only when both pmos is 0 and nmos is 1.

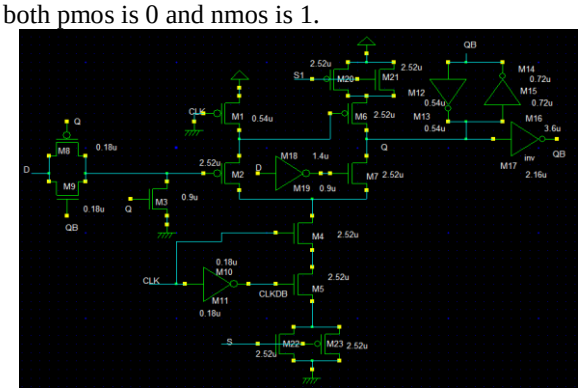

Fig.15 CPSFF Dual sleep

5.3.1 Simulation result Dual Sleep CPSFF
The CPSFF dual sleep circuit is simulated in HSPICE at level 64 with L=0.18u

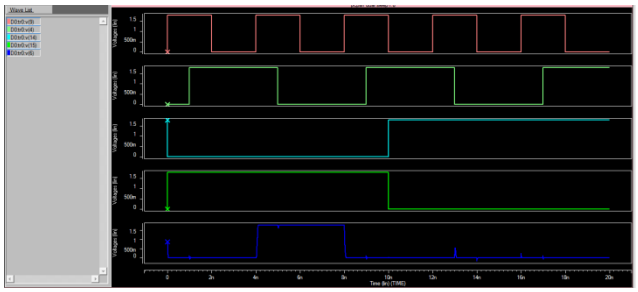

Fig.16 CPSFF Dual Sleep output Wave form

The control transistors in Dual sleep CPSFF saves the power when S1 is 1 and S is 0 from Fig.16

5.4 CPSFF Sleepy stack Approach

The sleepy stack[7] approach combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors The extra pair are arranged in pull up mode (M20, M21) and another pair in pull down mode (M23,M22) are arranged

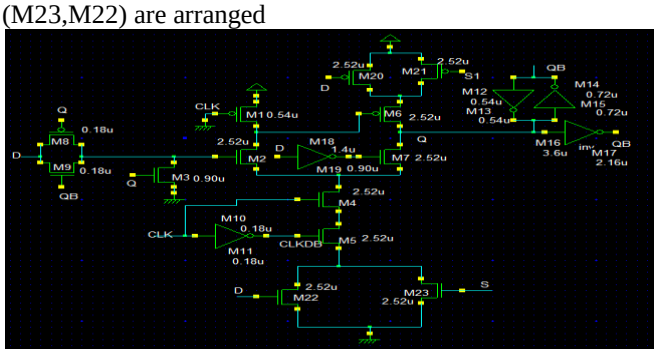

Fig.17 CPSFF Sleepy stack

5.4 Simulation result of Sleepy Stack CPSFF
The CPSFF sleepy stack circuit is simulated in HSPICE at level 64

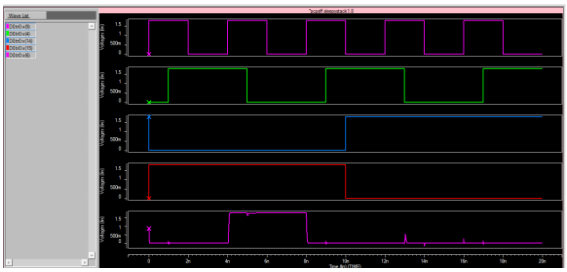

Fig.18 CPSFF Sleepy stack Wave form

The control transistors in Dual sleep CPSFF saves the power when S1 is 1 and S is 0 from Fig.18

VI. Simulation Results

The simulation results were obtained from HSPICE simulations in 0.18um CMOS technology at room temperature. VDD is 1.8 V. we have simulated the circuits in a real environment, where the flip-flop inputs (clock, data) are driven by the input buffers, and the output is required to drive an output load. An inverter is placed after output Q, providing protection from direct noise coupling [6].In order to calculate the delay COSMOSCOPE is used

In Fig .19 the CDMFF parameters with low power techniques are compared ,in dual sleep CDMFF the power saving is more and it is 55.5%

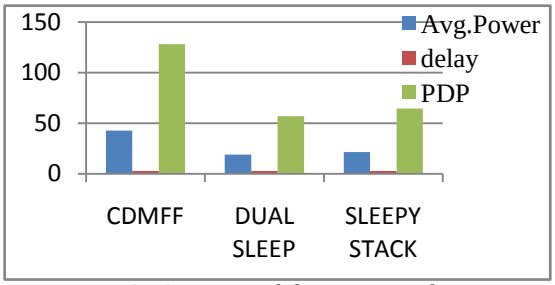

Fig.19 CDMFF with low power techniques

In Fig .20 the CPSFF parameters with low power techniques are compared, in dual sleep CDMFF the power saving is more and it is 49.019%

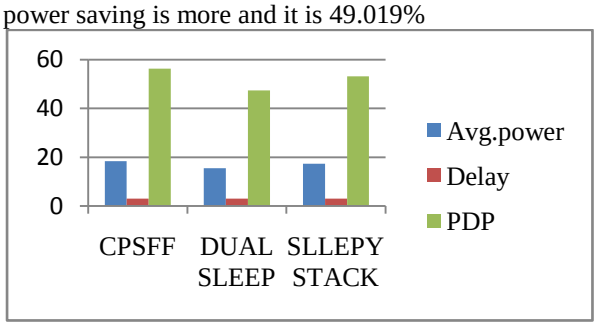

Fig.20 CPSFF with low power techniques

VII. Conclusion

In this paper, a variety of design techniques for low power clocking systems are proposed. One effective method is reducing the number of clocked transistors, is elaborated. Following the approach a novel clock pair shared flip flop is proposed, which reduces the power 12.84% compared to CDMFF.Static power is reduced by using dual sleep and sleepy stack approaches ,it reduces the static power effectively but increases the number of transistors so area of circuit increases. In future using the transmission gates and pass transistor logic, The number of transistors in flip flop is reduced. so area of circuit is decreased.

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ABOUT AUTHORS

Mr. S.Sasidhar Reddy pursing M.tech at Sri Venkateswera College of Technology(Autonomous) ,Chittoor ,A.P,India . His interested areas are Low Power VLSI and Digital Electronics and communication systems.

Mr.B.Shoban Babu received B.Tech Degree from, JNTUA, Anantapur,A.P, India and M.Tech from VTU, Belgum,, Karnataka, India. He is pursing PhD in Image Processing in S.V university, Tirupati,India.present working as a Associate professor at Sri Venkateswara college ofEng&Technology(Autonomous),Chitoor Dist,A.P .His interested areas are Digital Image processing and VLSI..He thought several subjects for under graduate and post graduate students